Polyphase Multifunction Energy Metering IC with Harmonic Monitoring

Silicon Anomaly

ADE7880

This anomaly list describes the known issues with the ADE7880 silicon identified by the version register (Address 0xE707) being equal to 1.

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ADE7880 FUNCTIONALITY ISSUES

Silicon Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Issues
Version = 1	ADE7880ACPZ	Released	Rev. A	4 (er001, er002, er003, er004)

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FUNCTIONALITY ISSUES

Table 1. LAST_ADD Register Shows Wrong Value for Harmonic Calculations Registers in SPI Mode [er001, Version = 1 Silicon]

Background	When any ADE7880 register is read using SPI or I^2C communication, the address is stored into LAST_ADD register.
Issue	When the harmonic calculation registers located between addresses 0xE880 and 0xE89F are read using SPI communication, LAST_ADD register contains the address of the register incremented by 1. The issue is not present if the I^2C communication is used.
Workaround	If LAST_ADD register is read after one of the registers located between addresses 0xE880 and 0xE89F was read using SPI communication, subtract 1 from it to recover the right address.
Related Issues	None.

Table 2. To Obtain Best Accuracy Performance, Internal Setting Must Be Changed [er002, Version = 1 Silicon]

Background	Internal default settings provide best accuracy performance for ADE7880.
Issue	It was found that if a different setting is used, the accuracy performance can be improved.
Workaround	To enable a new setting for this internal register, execute three consecutive write operations: The first write operation is to an 8-bit location: 0xAD is written to Address 0xE7FE. The second write operation is to a 16-bit location: 0x3BD is written to Address 0xE90C. The third write operation is to an 8-bit location:0x00 is written to Address 0xE7EF. The write operations must be executed consecutively without any other read/write operation in between. As a verification that the value was captured correctly, a simple 16-bit read of address 0xE90C should show the 0x3BD value.
Related Issues	None.

Table 3. High Pass Filter Cannot be Disabled in Phase C Voltage Data Path [er003, Version = 1 Silicon]

Background	When Bit 0 (HPFEN) of the CONFIG3 register is 0, all high-pass filters (HPF) in the phase and neutral currents and phase voltages data paths are disabled (see the ADE7880 data sheet for more information about the current channel HPF and the voltage channel HPF).
Issue	The HPF in the phase C voltage data path remains enabled independent of bit HPFEN state.
Workaround	There is no workaround.
Related Issues	None.

Table 4. No Load Condition Does Not Function as Defined [er004, Version = 1 Silicon]

Background	Total active power no load uses the total active energy and the apparent energy to trigger the no load condition. If neither total active energy nor apparent energy are accumulated for a time indicated in the respective APNOLOAD and VANOLOAD unsigned, 16-bit registers, the no load condition is triggered, the total active energy of that phase is not accumulated and no CF pulses are generated based on the total active energy. Fundamental active and reactive powers no load uses the fundamental active and reactive energies to trigger the no load condition. If neither the fundamental active energy nor the fundamental reactive energy are accumulated for a time indicated in the respective APNOLOAD and VARNOLOAD unsigned 16-bit registers, the no load condition is triggered, the fundamental active and reactive energies of that phase are not accumulated, and no CF pulses are generated based on the fundamental active and reactive energies.
Issue	When the total active energy on Phase x (x = A, B, or C) is lower than APNOLOAD and the apparent energy is above VANOLOAD, the no load condition should not be triggered. It was observed that although CF pulses continue to be generated, the Bit 0 (NLOAD) and Bits[2:0] (NLPHASE) in STATUS1 and PHNOLOAD registers continue to be cleared to 0 indicating an out of no load condition, the xWATTHR register stops accumulating energy. It was observed that the fundamental active energy no load functions independently of the fundamental reactive energy no load. If, for example, the fundamental active energy is below APNOLOAD and the fundamental reactive energy is above VARNOLOAD, both energies should continue to accumulate because the phase is out of no load condition. Instead, the CF pulses, based on the phase fundamental active energy, are not generated and the FWATTHR registers are blocked, while the CF pulses, based on the fundamental reactive energy, are generated. Thus, the FVARHR registers continue to accumulate and the Bit 1 (FNLOAD) in the STATUS1 register and Bits[5:3] (FNLPHASE) in the PHNOLOAD register are cleared to 0.
Workaround	Because both no load conditions use the APNOLOAD threshold, a workaround for both issues is presented as follows: • Clear APNOLOAD and VARNOLOAD to 0. • Set VANOLOAD at desired value. When the Phase x (x = A, B, or C) apparent energy becomes smaller then VANOLOAD, the Bit 2 (VANLOAD) in STATUS1 is set to 1, together with one of the Bits[2:0] (VANLPHASE) in PHNOLOAD. Then, set APNOLOAD and VARNOLOAD equal to VANOLOAD. The Phase x (x = A, B, or C) total active energy enters no load condition. • CF pulses stop. • Bit 0 (NLOAD) in the STATUS1 register is set to 1. • One of the Bits[2:0], (NLPHASE[2:0]), in the PHNOLOAD register is set to 1. • The xWATTHR register stops accumulating energy. The Phase x (x = A, B, or C) fundamental active and reactive energies enter no load condition. • CF pulses stop. • Bit 1 (FNLOAD) in the STATUS1 register is set to 1. • One of the Bits[5:3], (FNLPHASE[2:0]), in the PHNOLOAD register is set to 1. • The xFWATTHR and xVARHR registers stop accumulating energy.
Related Issues	None.

SECTION 1. ADE7880 FUNCTIONALITY ISSUES

Reference Number	Description	Status
er001	LAST_ADD register shows wrong value for harmonic calculations registers in SPI mode.	Identified
er002	To obtain best accuracy performance, internal setting must be changed.	Identified
er003	High-pass filter cannot be disabled in phase c voltage data path.	Identified
er004	No load condition does not function as defined.	Identified

NOTES

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